

LATCHING MICRO MAGNETIC RELAY PACKAGES
AND METHODS OF PACKAGING

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application Serial Number 60/322,841, entitled MICRO MAGNETIC SWITCH FABRICATION AND APPARATUS, filed 17 September 2001.

Field of the Invention

This invention relates to latching micro magnetic relays.

More particularly, the present invention relates to methods of packaging latching micro magnetic relays and the various packages.

Background of the Invention

Recently, novel latching micro magnetic relays were discovered. The novel latching micro magnetic relay is

1 based on preferential magnetization of a soft magnetic
2 cantilever in a permanent external magnetic field.
3 Switching between two magnetic states is accomplished by
4 momentarily changing the direction of the cantilever's
5 magnetization by passing a short current pulse through a
6 planar coil situated adjacent the cantilever. Once the
7 relay is switched, it is held in this nonvolatile state
8 (latched) by the permanent external magnetic field.
9 Additional information as to the construction and operation
10 of the novel latching micro magnetic relay is disclosed in a
11 copending United States patent application entitled
12 "Electronically Switching Latching Micro-Magnetic Relay and
13 Method of Operating Same", with serial number 09/496,446,
14 filing date 02 February 2000, and incorporated herein by
15 reference. While a specific latching micro magnetic relay
16 is described above, it will be understood that other Micro
17 Electro Mechanical Systems (MEMS) devices that incorporate
18 magnets are also included in this description.

19

20 In the prior art, the cantilever for micro magnetic
21 switches was fabricated as a complete portion of the switch
22 by providing a sacrificial layer of photoresist, depositing
23 the material of the cantilever on the surface of the
24 photoresist and then etching or otherwise dissolving the
25 photoresist layer to provide a cantilever. One problem with

1 this prior art method is that any process steps performed
2 subsequent to the application of the photoresist layer are
3 seriously limited because of potential damage to the
4 photoresist material and, thus, potential faults or
5 weaknesses in the final product.

6
7 Also, in most prior art packaging techniques relatively
8 high temperatures are required for some of the later steps.
9 These high temperatures can seriously affect magnets and
10 some of the other components enclosed in the packages.
11 Further, the materials that could be used as the supporting
12 substrate for the MEMS devices is seriously limited by the
13 fabrication and packaging techniques.

14
15 It would be highly advantageous, therefore, to remedy
16 the foregoing and other deficiencies inherent in the prior
17 art.

18
19 Accordingly, it is an object the present invention to
20 provide a new and improved latching micro magnetic relay and
21 package.

22
23 Another object of the present invention is to provide a
24 new and improved latching micro magnetic relay package that
25 can be fabricated on a variety of substrates.

1 Another object of the present invention is to provide a
2 new and improved latching micro magnetic relay package that
3 is easy and inexpensive to manufacture.

4

5 A further object of the present invention is to provide
6 a new and improved latching micro magnetic relay package
7 fabricated with low temperature assembly.

8

9 Still another object of the present invention is to
10 provide a new and improved latching micro magnetic relay
11 package that can be hermetically sealed on any of a variety
12 of improved substrates using relatively low temperature.

1 Summary of the Invention

2

3 Briefly, to achieve the desired objects of the present

4 invention in accordance with a preferred embodiment thereof,

5 provided is a method of forming a package and sealing a MEMS

6 device in the package including the steps of providing a

7 supporting substrate, forming at least one contact for the

8 MEMS device on the surface of the supporting substrate and

9 providing an external connection to the contact, forming a

10 cantilever on the surface of the supporting substrate, the

11 cantilever being positioned to come into electrical

12 engagement with the contact in one orientation, and

13 depositing a seal ring on the surface of the supporting

14 substrate circumferentially around the contact and the

15 cantilever. The method further includes the steps of

16 forming a cap member with a cavity and a continuous edge

17 circumferentially around the cavity, the cavity being

18 designed to receive the cantilever and contact therein, and

19 depositing a seal ring on the continuous edge of the cap

20 member. The package is then sealed by sealingly engaging

21 the seal ring on the continuous edge of the cap member to

22 the seal ring on the surface of the supporting substrate.

23

24 In a preferred and more specific embodiment, the sealed

25 package includes a supporting substrate with a surface, at

1 least one contact for the MEMS device on the surface of the
2 supporting substrate with an external connection to the
3 contact and a cantilever on the surface of the supporting
4 substrate, the cantilever being positioned to come into
5 electrical engagement with the contact in one orientation.
6 A metal seal ring is fixed on the surface of the supporting
7 substrate circumferentially around the contact and the
8 cantilever. A cap member is formed with a cavity and a
9 continuous edge circumferentially around the cavity. The
10 cavity is designed to receive the cantilever and contact
11 therein with the continuous edge in mating engagement with
12 the metal seal ring on the surface of the supporting
13 substrate. A metal seal ring is fixed on the continuous
14 edge of the cap member. The metal seal ring on the
15 continuous edge of the cap member is sealingly engaged with
16 the metal seal ring on the surface of the supporting
17 substrate. In the preferred embodiment the two metal seal
18 rings are sealingly engaged or fixed together by a solder
19 alloy that is reflowed in an inert environment without the
20 use of flux.

1 Brief Description of the Drawings

2
3 The foregoing and further and more specific objects and
4 advantages of the invention will become readily apparent to
5 those skilled in the art from the following detailed
6 description of a preferred embodiment thereof, taken in
7 conjunction with the drawings in which:

8
9 FIG. 1 is a simplified sectional view illustrating one
10 embodiment of a wafer scale packaging process for a latching
11 micro magnetic relay;

12
13 FIG. 2 is a view in top plan of a pair of wafer as used
14 in the present invention;

15
16 FIG. 3 is a simplified sectional view of the wafers of
17 FIG. 2 in alignment, prior to bonding;

18
19 FIG. 4 is a more detailed and enlarged sectional view
20 of the wafers of FIG. 2 in alignment, prior to bonding;

21
22 FIG. 5 is a more detailed and enlarged sectional view
23 of the wafers of FIG. 4 in alignment, subsequent to bonding;

1 FIG. 6 is a view in top plan of a portion of the bonded
2 wafers prior to dicing;

3
4 FIG. 7 is an enlarged sectional view of a single
5 package after dicing; and

6
7 FIG. 8 is a simplified sectional view illustrating
8 portions of another embodiment of a wafer scale packaging
9 process for a latching micro magnetic relay.

1 Detailed Description of a Preferred Embodiment

2
3 Turning now to FIG. 1, a wafer scale package 10 is
4 illustrated for a latching micro magnetic relay or other
5 MEMS structures incorporating a magnet or other heat
6 sensitive components. As will be described in more detail
7 below, one major advantage of package 10 is that it can be
8 assembled using solder preforms and low temperature
9 assembly. Low temperature assembly is desirable because the
10 magnet incorporated in the MEMS structure can easily be
11 damaged by too much heat.

12
13 As will become apparent from the discussion below,
14 package 10 can be fabricated in wafer format and does not
15 require the assembly of the MEMS devices individually into
16 individual packages. As described in conjunction with the
17 above structure, a plurality of MEMS devices are generally
18 formed simultaneously on a single wafer. If the wafer must
19 be separated into individual MEMS devices and each
20 individual device packaged separately, the labor cost
21 becomes very high.

22
23 In this specific embodiment, a GaAs substrate 12 is
24 used but it should be understood that the substrate could be
25 formed of silicon, glass, quartz, or any other convenient
26 material that provides the desired characteristics, such as

1 any of the well known semiconductor material, such as
2 silicon, gallium arsenide, etc., or it can include quartz
3 ceramics, various organic or magnetic materials, etc.
4 Generally, as will be understood by those skilled in the
5 art, a GaAs substrate is preferred because the material
6 provides substantial benefits at higher frequencies.
7 However, the art of silicon processing has developed to a
8 very advanced state in the semiconductor field and is,
9 therefore, very useful in the present invention. Also, in
10 some specific applications, cooperating or externally
11 connected circuitry can be formed directly on the same
12 substrate to reduce connection losses. As will be explained
13 in more detail presently, substrate 12 is generally included
14 as a small portion of a much larger wafer, the individual
15 packages 10 being separated only after substantial portions
16 of the fabrication are completed.

17
18 In this preferred embodiment, a pair of vias 14 are
19 provided in substrate 12 and can be formed by any of a
20 variety of well known processes including etching, laser
21 drilling, etc. Generally, the method of formation of vias
22 14 is determined by the cost of the different procedures.
23 Also, vias 14 are plugged or filled with a conductive
24 material. Technology for plugging or filling vias 14 in
25 GaAs, silicon, or glass exists and will not be elaborated

1 upon in this disclosure. The lower or external portions of
2 vias 14 are barrier plated for solderability to allow solder
3 bumping or direct solder attachment to a printed wiring
4 board, ceramic board, etc. Also, the lower or external
5 portions of vias 14 form an I/O interface which in the
6 finished format allow for the clearance of the finished
7 package off the surface of a mounting board (not shown).

8

9 In general, once vias 14 in substrate 12 are plugged,
10 fabrication of a MEMS device 15 on substrate 12 proceeds in
11 a normal fashion. Because virtually any type of MEMS device
12 can be incorporated into package 10, MEMS device 15 is
13 represented in FIG. 1, simply by a cantilever 16 positioned
14 to provide a contact between spaced apart conductive pads 17
15 and 18 in an activated state. A hermetic seal ring 20A is
16 positioned around each MEMS device 15 on the wafer
17 (substrate 12). Because a plurality of packages 10 are
18 formed simultaneously on a common wafer, seal rings 20A are
19 all patterned on the wafer surface using common patterning
20 steps.

21

22 Seal ring 20A is preferably metallized onto the
23 surface of wafer 12 and generally includes a thin portion or
24 layer (an adhesion layer) of material or metal that adheres
25 well to wafer 12 (e.g. tungsten, titanium, or combinations

1 thereof) and a thicker portion or layer (a sealing layer) of
2 a sealing or junction material, e.g., nickel/gold,
3 chrome/gold, etc. Generally, at least a 0.5 mm seal ring
4 20A around each MEMS device 15 is provided for a hermetic
5 seal. Also, provisions are included for a saw kerf between
6 adjacent die when the wafer is separated into individual
7 packages. A disadvantage is that seal ring 20A and the saw
8 kerf use substantial wafer area, but various procedures and
9 alterations may be incorporated to minimize this problem.

10

11 A silicon wafer is provided to form a hermetic cap 22
12 to be incorporated with a seal ring 20B. While a single cap
13 22 is illustrated it will be understood that a number of
14 caps will be formed in the silicon wafer equal to the number
15 of MEMS devices formed in the GaAs wafer. Again it will be
16 understood that hermetic cap 22 could be formed from other
17 material, such as glass, ceramic, etc. but silicon is used
18 in this preferred embodiment because of the vast knowledge
19 and machinery available for working with silicon.
20 Anisotropic etching of vias, holes grooves, etc. in silicon
21 wafers is a reasonably well understood process.

22

23 A silicon wafer of the right thickness to house a
24 magnet 24 and to clear cantilever 16 of MEMS device 15 is
25 selected. Holes, e.g. circular, square, etc., are etched in

1 the silicon wafer on a precise pitch. The precise pitch is
2 of course the same pitch used to form MEMS devices 15 and
3 seal rings 20A on the GaAs wafer (substrate 12). Seal ring
4 20B is metallized on the lower lips of each cap 22 and
5 formed generally as described for seal ring 20A above. To
6 allow a hermetic sealing of cap 22 to substrate 12 an 80/20
7 Au/Sn preform is tack welded to either metallized seal ring,
8 that is seal ring 20A on substrate 12 or seal ring 20B on
9 cap 22. In another method, 80/20 Au/Sn alloy can be plated
10 on seal ring 20B of cap 22. In this procedure, plating the
11 alloy on the seal ring is believed to be more variable than
12 using a tacked preform.

13

14 At any convenient time during the fabrication, a magnet
15 24 is aligned and bonded (e.g. by epoxy or other suitable
16 adhesive) into the cavity in each cap 22 of the silicon
17 wafer. To this end, using machine vision allows magnets 24
18 to be precisely placed in the center of each cavity. It
19 will be understood that, in some specific applications,
20 magnet 24 can be placed outside of the package, if desired.

21

22 The anisotropically etched caps 22 on the silicon wafer
23 are aligned to the MEMS device on the GaAs wafer and
24 hermetically sealed by reflowing the 80/20 Au/Sn alloy in an
25 inert environment without the use of any flux. Thus, metal

1 seal ring 20A and metal seal ring 20B are affixed together
2 to form a compound seal ring 20. An appropriate
3 fiducial/alignment scheme can be developed for the wafers to
4 ensure each magnet 24 is aligned to within +/- .001" of the
5 center of each and every MEMS device 15.

6

7 The coefficient of thermal expansion of silicon is 2.3
8 - 4.7 (ppm/C) and for GaAs is 5.4 - 5.72 (ppm/C). There
9 thus would be a minimal mismatch in the coefficient of
10 thermal expansion of about 2 (ppm/C). The consequence of
11 this mismatch is that if stress problems arise in specific
12 application, an Au/Sn alloy which is some what more tin rich
13 could be used to provide the stress relief. In applications
14 where the substrate and cap are formed of similar material
15 thermal expansion is not a problem. The use of other lower
16 temperature solder is possible in all cases as long as
17 fluxless soldering processes are used.

18

19 While the above structure provides a complete hermetic
20 seal for the micro magnetic relay or other MEMS structure,
21 it will be understood that in some applications such
22 hermeticity is or may not be required. Thus, in such
23 applications instead of the metal seal rings and/or the
24 solder, the cap may simply be epoxied or otherwise adhered

1 to the substrate or the seal rings may be epoxied or adhered
2 together.

3
4 Finally, a permalloy backing sheet 25 (magnetic flux
5 concentrator) is bonded to the I/O side of the hermetically
6 sealed wafer scale package 10. Permalloy backing sheet 25
7 is preferably of a grillage format to allow bonding of all
8 sites (i.e. all packages 10 on the GaAs wafer) at once. The
9 exposed surface of permalloy backing sheet 25 preferably is
10 provided with an organic dielectric coating. The dielectric
11 coating ensures that no electric paths develop between the
12 external portions of vias 14 or any conductors on the
13 surface of the mounting board. The bonded side of permalloy
14 backing sheet 25 preferably has a pressure sensitive
15 thermally cureable adhesive thereon. By supplying a
16 pressure sensitive adhesive on permalloy backing sheet 25
17 assembly can be accomplished very easily.

18
19 Generally, an advantage of wafer scale packages 10 is
20 that they can be tested in wafer format (i.e. before
21 separation into individual parts) and then the wafer can be
22 solder bumped if desired. The wafer is then sawn, or
23 otherwise separated, to provide singulated components.
24 Alternatively, the wafer could be sawn to provide singulated
25 components and then tested and individually solder bumped if

1 desired. Implicit in this procedure is that the wafer die
2 yield is very high (approximately +98%).

3
4 Turning now to FIG. 2, a pair of wafers 30 and 32
5 (device and encapsulation wafers, respectively) are
6 provided. Here it will be understood that wafers 30 and 32
7 can include any of the well known semiconductor material,
8 such as silicon, gallium arsenide, etc., or they can include
9 quartz ceramics, various organic or magnetic materials, etc.
10 Referring additionally to FIG. 3, it can be seen that an
11 array of latching micro magnetic relays or other MEMS
12 structures are formed on wafer 30 and a similar array of
13 caps are formed in wafer 32. Wafers 30 and 32 are axially
14 aligned in overlying relationship so that a cap in wafer 32
15 overlies each latching micro magnetic relay or other MEMS
16 structure on wafer 30.

17
18 Referring additionally to FIG. 4, an enlarged more
19 detailed sectional view is illustrated of wafers 30 and 32.
20 From this view it can be seen that magnets 34 are positioned
21 in the upper surface of wafer 32 and aligned, one each, with
22 cavities 35 in the lower surface of wafer 32. Wafers 30 and
23 32 are then brought together and bonded, as illustrated in
24 FIG. 5. Thus, an array of wafer scale packages are
25 manufactured simultaneously in wafers 30 and 32, as

1 illustrated in FIG. 6. The bonded wafers are then diced, or
2 otherwise separated into a plurality of wafer scale
3 packages. A single one of the wafer scale packages,
4 designated 40, is illustrated in an enlarged sectional view
5 in FIG. 7. The individual packages can be tested before
6 dicing and/or after dicing if desired.

7

8 Turning now to FIG. 8, one way to save some of the area
9 required for hermetically sealing wafer scale MEMS package
10 10 is illustrated. In this procedure, the package is
11 modified from a single plane layout to a multilayer layout.
12 In the multilayer layout of FIG. 8, the structure includes a
13 substrate 50, a permalloy layer 52, a ground plane 54, an
14 insulating dielectric layer 56, and a layer 58 for RF
15 routing and coils. Here it is also assumed the the MEMS
16 cantilever (not shown) is mounted in the same plane as the
17 RF lines. Ground plane 54 is formed of electrically
18 conductive but non-magnetic material (e.g. gold or the like)
19 so as not to reduce the effects of permalloy layer 52.
20 Also, capacitance coupling effects can be mitigated by
21 controlling the thickness of dielectric layer 56.

22

23 The structure described above can save wafer space but
24 will include additional mask layers and fabrication steps.
25 A polymer dielectric that can be used in lieu of polyimide

1 and has RF potential because of its low loss, is Dow
2 Chemical's benzocyclobutene (BCB). This material has been
3 used extensively for high density interconnects in multi
4 chip modules. Another possible high frequency dielectric
5 that can be used is one of the formulations of nitride which
6 is inorganic.

7
8 Thus, a new and improved latching micro magnetic relay
9 or MEMS package has been disclosed, which is highly
10 adaptable and easy to manufacture. Also, the improved
11 package and methods of fabrication can incorporate a variety
12 of different supporting substrates. Further, a variety of
13 different caps can be easily fabricated and applied to the
14 substrate using low temperature processes. Because the
15 preferred manufacturing process contemplates the
16 simultaneous fabrication of a plurality of packages on a
17 single wafer, the packages can be tested at various points
18 during the manufacturing process and defective packages can
19 be eliminated before too much time and resources are
20 expended.

21
22 Various changes and modifications to the embodiments
23 herein chosen for purposes of illustration will readily
24 occur to those skilled in the art. To the extent that such
25 modifications and variations do not depart from the spirit

1 of the invention, they are intended to be included within
2 the scope thereof, which is assessed only by a fair
3 interpretation of the following claims.

4

5 Having fully described the invention in such clear and
6 concise terms as to enable those skilled in the art to
7 understand and practice the same, the invention claimed is: